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Claims

[c1] A field effect transistor (FET) comprising:
a thin channel having a first thickness;
a gate disposed above said thin channel;
a source/drain region in a recess at each end of said thin channel and substantially thicker than said thin channel; and
a source/drain extension between said thin channel and a corresponding said source/drain region, each said source/drain extension and said corresponding source/drain region being aligned to said gate and said thin channel.

[c2] An FET as in claim 1, wherein said recess extends under said gate at said each end.

[c3] An FET as in claim 1, wherein said recess partially extends under said gate at said each end.

[c4] An FET as in claim 1, wherein an upper surface of each said source/drain region is substantially coplanar with an upper surface of said thin channel.

[c5] An FET as in claim 1, wherein said thin channel is a semiconductor material selected from a group consisting

of silicon (Si), Germanium (Ge), SiGe and strained silicon (SSi).

[c6] An FET as in claim 5, wherein said thin channel is strained silicon.

[c7] An FET as in claim 5, wherein said gate is made from a material comprising polysilicon.

[c8] An FET as in claim 5, wherein said gate is made from a material comprising a silicide.

[c9] An FET as in claim 1, wherein said thin channel is smaller than 15nm thick.

[c10] An FET as in claim 9, wherein said thin channel is 10nm thick.

[c11] An FET as in claim 9, wherein said thin channel is smaller than 40nm long.

[c12] An FET as in claim 11, wherein said thin channel is 30nm long.

[c13] An FET as in claim 9, wherein a lower surface of said recess is greater than 5nm below said thin channel.

[c14] An FET as in claim 13, wherein said lower surface is 40nm below said thin channel.

[c15] An FET as in claim 1, wherein said FET is disposed on an insulating layer and said insulating layer is disposed on a semiconductor substrate.

[c16] An FET as in claim 15, wherein said semiconductor substrate comprises a silicon substrate.

[c17] An FET as in claim 15, wherein said semiconductor substrate comprises a strained silicon/silicon germanium (SSi/SiGe) substrate.

[c18] An integrated circuit (IC) on a silicon on insulator (SOI) chip, said IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, said insulating layer being on a semiconductor substrate, each of said FETs comprising:
a thin channel, said thin channel being a thin semiconductor layer and having a first thickness;
a gate disposed above said thin channel;
a source/drain region in a recess at each end of said thin channel and substantially thicker than said thin channel; and
a source/drain extension between said thin channel and a corresponding said source/drain region, each said source/drain extension and said corresponding source/drain region being aligned to said gate and said thin channel.

[c19] An IC as in claim 18, wherein each said recess extends under a corresponding said gate at said either end.

[c20] An IC as in claim 18, wherein each said recess partially extends under a corresponding said gate at said either end.

[c21] An IC as in claim 18, wherein said thin semiconductor layer is a layer of material selected from a group consisting of silicon (Si), Germanium (Ge), SiGe and strained silicon.

[c22] An IC as in claim 21, wherein said thin channel is silicon and said gate is polysilicon.

[c23] An IC as in claim 22, wherein said thin channel is strained silicon.

[c24] An IC as in claim 22, wherein said thin channel is < 15nm thick.

[c25] An IC as in claim 24, wherein a lower surface of each said recess is greater than 5nm below said thin channel

[c26] An IC as in claim 25, wherein said thin channel is smaller than 40nm long.

[c27] An IC as in claim 26, wherein said semiconductor substrate is a silicon substrate.

[c28] An IC as in claim 27, wherein said semiconductor substrate is a strained silicon/silicon germanium (SSi/SiGe) substrate.

[c29] A method of forming an integrated circuit (IC), said method comprising the steps of:
a) defining device regions on a silicon on insulator (SOI) wafer;
b) defining source/drain areas at opposite sides of a gate in each of said device regions;
c) undercutting source/drain areas; and
d)filling undercut said source/drain areas with silicon, filled said undercut forming source/drain regions and extensions, a device channel being defined beneath each said gate self aligned to pairs of said source/drain regions and extensions.

[c30] A method of forming an IC as in claim 29, wherein the SOI wafer is a bonded SOI wafer having an ultra-thin silicon layer and a semiconductor substrate, said ultra-thin silicon layer being smaller than 10nm thick, the step (a) of defining device regions comprising the steps of:
i) forming gates on said ultra-thin silicon layer;
ii) forming trenches around device areas, said trenches being formed through said ultra-thin layer to said semiconductor substrate; and

iii) filling said trenches with an insulating material.

[c31] A method of forming an IC as in claim 30, wherein the step (b) of defining said source drain areas comprises forming a void between said ultra-thin silicon layer and said semiconductor substrate.

[c32] A method of forming an IC as in claim 31, wherein the SOI wafer further includes a sacrificial layer between said ultra-thin silicon layer and said semiconductor substrate and the step (a) of defining device regions further comprises the step of:
iv) implanting a dopant into said sacrificial layer.

[c33] A method of forming an IC as in claim 32, wherein said gates block said dopant implanted in implanting step (a)(iv), undoped portions of said sacrificial layer remaining beneath said gates.

[c34] A method of forming an IC as in claim 33, wherein the SOI wafer further includes an insulating layer between said sacrificial layer and said semiconductor substrate and forming said void in step (b) comprises the steps of:
i) opening orifices through said ultra-thin silicon layer to said semiconductor substrate at each end of each of said devices regions;
ii) removing portions of said insulating layer in said de-

vice areas between said orifices; and
iii) removing said undoped portions of said sacrificial layer, remaining doped portions of said sacrificial layer defining said source/drain areas.

[c35] A method of forming an IC as in claim 34, wherein the step (c) of undercutting the source/drain areas comprises the steps of:
i) filling said void with an insulating material, said insulating material at least partially filling said orifices such that at least the bottom of said remaining doped portions is below an upper surface of said fill insulating material;
ii) removing remaining said doped portions; and
iii) exposing an underside of said ultra-thin silicon layer above removed said doped portions.

[c36] A method of forming an IC as in claim 35, wherein said insulating layer fills said orifices and the step (c)(i) further comprises etching said insulating material back.

[c37] A method of forming an IC as in claim 36, wherein remaining said doped portions are doped with a first dopant type and the step (c)(ii) of removing remaining said doped portions comprises:
A) implanting a second dopant type into remaining said doped portions;

B) annealing said SOI wafer, remaining said doped portions changing semiconductor type to said second type; and

C) selectively etching with an etchant selective to said second type.

[c38] A method of forming an IC as in claim 37, wherein the step (d) of filling said undercut source/drain and extension areas comprises growing silicon epitaxially in said undercut source/drain areas, said epitaxially grown silicon growing from said ultra-thin silicon layer and filling said undercut source/drain areas, a recessed extension and source/drain being formed by said epitaxially grown silicon and said ultra-thin silicon layer at each end of said self aligned channel.